State-Preserving Intermittently Locked Loop (SPILL) Frequency Synthesizer for Portable Radio

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Abstract—A novel PLL concept, SPILL, suitable for the intermittent operation of frequency synthesizers used in UHF portable radio sets is proposed. SPILL employs a new digital circuit technique which preserves frequency and phase during power-off periods, in order to perform fast acquisition at the beginning of power-on periods. Both a theoretical analysis and experiments confirm acceptable acquisition performance. A 1.6 GHz SPILL frequency synthesizer achieves an improvement in acquisition time by two orders of magnitude. Applications of SPILL to high-frequency synthesizers in portable radio communication sets are especially effective for reducing power consumption.

I. INTRODUCTION

IN MOBILE RADIO communications, reducing power consumption of UHF portable radio communication sets is an extremely important subject [1], [2]. This paper focuses on power saving by intermittent operation of the phase-locked-loop (PLL) frequency synthesizer, which has the highest power consumption in the receiver circuit. In this intermittent operation, power to the whole synthesizer circuit, including the VCO, is supplied intermittently. It is suitable for mobile radio systems where the data signals for a receiver are transmitted intermittently and the receiver does not need to receive the other parts of the signal [1]. Intermittent receiver operation for reducing power consumption has proved to be effective in paging systems.

The effectiveness of power reduction by introducing the above intermittent operation largely depends upon the ratio of power-on to power-off periods. The smaller the ratio, the more effective the operation. However, the decrease in ratio has been limited by the frequency acquisition time of the PLL phase lock process. To further reduce power consumption by intermittent operation, extremely fast frequency acquisition at the beginning of the power-on stage must be realized.

This acquisition time has been shortened by employing a dual-mode loop filter which uses a short time constant in the establishment period of phase lock only and then changes to a long time constant [3]. This technique cannot reduce the period of the phase lock process enough to achieve further power reduction. Moreover, it is accompanied with large frequency fluctuations, which are unacceptable in a radio communication system. For solving these problems, a novel PLL concept, the state-preserving intermittently locked loop (SPILL), which preserves the state (phase and frequency) of the PLL during the power-off stage, is proposed. For phase state preserving, an "initial-phase adjustment" technique is developed. If frequency and phase differences between the VCO output signal and the reference signal are reduced to nearly zero by the state-preserving technique, the phase lock establishment process can be reduced to less than one hundredth of the original value.

In this paper, an initial-phase adjustment circuit implemented with a digital circuit is presented for the SPILL frequency synthesizer. The circuit employs a newly developed resettable high-speed prescalar as a variable VCO frequency divider. The resettable function allows phase adjustment at the beginning of the power-on state with one-period precision of the VCO oscillation frequency. The performance of the SPILL frequency synthesizer in a 1.6 GHz band is shown theoretically and confirmed experimentally. The experiments demonstrate a very short frequency acquisition time (less than 1 ms) and extremely small frequency fluctuations at the beginning of the power-on state. Consequently, power wasted in intermittent operation is very small, and this synthesizer has the great advantage of significantly reduced power consumption.

II. PRINCIPLE OF SPILL

A. Intermittent Operation

A general control sequence of intermittent operations against a transmitted multiplexed paging signal from a base station is shown in Fig. 1. Only during periods when the required information is transmitted in the paging signal is power supplied to the receiver. In the power-on state, power to the whole synthesizer circuit is supplied. In the power-off state, power is not supplied to any part of the synthesizer circuit. The intermittent ratio is defined as the ratio of power-on to power-off periods. The smaller the intermittent ratio, the shorter the power supply time and the smaller the power consumption. For UHF band applications, it takes tens of milliseconds for phase lock estab-

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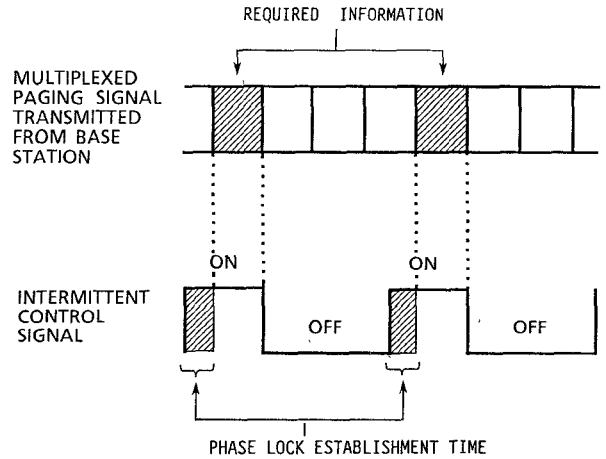

Fig. 1. Control sequence of intermittent operation.

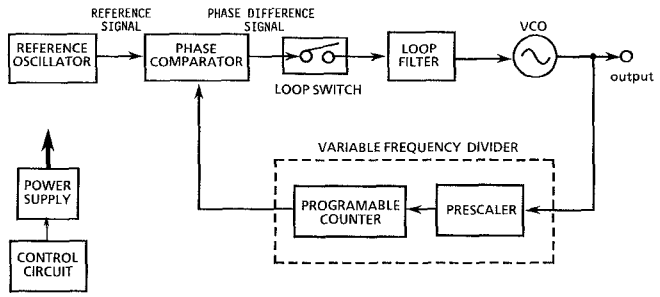

Fig. 2. Configuration of a conventional synthesizer.

lishment after power-on. Consequently, power should be supplied earlier by a time equivalent to this phase lock establishment. For intermittent operation, the phase lock establishment time should be much shorter than the power-on period to increase the effectiveness of power reduction.

B. Principle of SPILL

The configuration of a conventional frequency synthesizer is shown in Fig. 2. The output signal from the variable frequency divider, in which the VCO output signal is divided to the same frequency as the reference signal, and the reference signal are applied to a phase comparator. The output of the comparator is a function of the phase difference between the two input signals. The comparator output is regulated by a loop filter, and is applied to the VCO input so that the VCO output signal phase is synchronized with the reference signal phase. If the VCO output signal and the reference signal retain this synchronous state, the VCO oscillation is characterized by the same stability as the reference signal.

The PLL state can be represented by its phase and frequency. Therefore, if its states of phase and frequency are preserved during the power-off stage, at the beginning of the power-on stage, the previous PLL states can be recovered in a very short time without frequency fluctuation. This new PLL concept is embodied in the SPILL synthesizer.

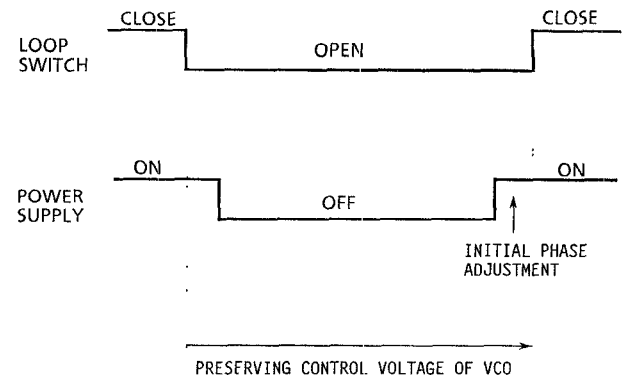

Fig. 3. Control sequence of intermittent operation.

Fig. 3 shows the intermittent operation sequence in the SPILL frequency synthesizer. First, to preserve the frequency state during the power-off stage, just before power-off the phase difference voltage from the phase comparator to the VCO is interrupted by opening the loop switch. Next, the power supply to each circuit is turned off for the same specified period of time. After the inactive period is finished, the power is resupplied to all circuits. At this point the initial phase of the output signal from the variable frequency divider is adjusted to the phase of the reference signal and any phase difference is removed. Once this adjustment is complete, the loop switch is closed and the phase difference is stabilized within one period of the UHF band VCO signal. This technique is called the initial-phase adjustment technique. The performance of this technique with actual digital circuits was confirmed. Further information about this technique will be given in Section III.

C. Analysis of Phase Lock Process in SPILL

If, after the loop is closed, there is an extremely small phase difference for the initial-phase adjustment, it is assumed that the phase locking process can be investigated as a frequency stepping response or a phase stepping response [4]. In reality, there are many cases where there is a simultaneous difference for both the frequency and the phase. In this report two cases, 1) when a frequency difference exists for zero phase difference (frequency stepping response) and 2) when a phase difference exists for zero frequency difference (phase stepping response), are analytically investigated. In this analysis, frequency transitional profiles at phase or frequency stepping response and phase lock establishment time are simulated.

The feedback circuit used in this investigation is composed of a digital type of phase comparator, a lag–lead type loop filter, and a charge pump which transmits phase difference signals from the phase comparator to the loop filter. In this feedback circuit, the charge pump output has three states: an open-loop state for the phase locked condition, and charging and discharging states of the loop filter when there is a large phase difference in the phase comparator. Therefore, the phase locking process is identified by the behavior of the PLL using a fully integrated filter; i.e., the PLL charge pump is of the current source type.

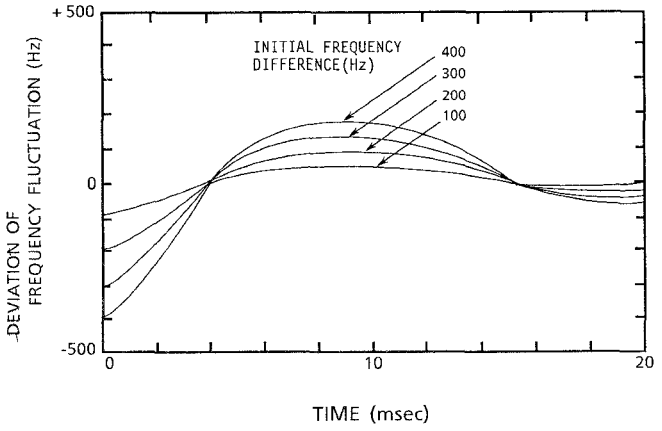

Fig. 4. Frequency response profiles for frequency stepping in the 1.6 GHz band synthesizer.

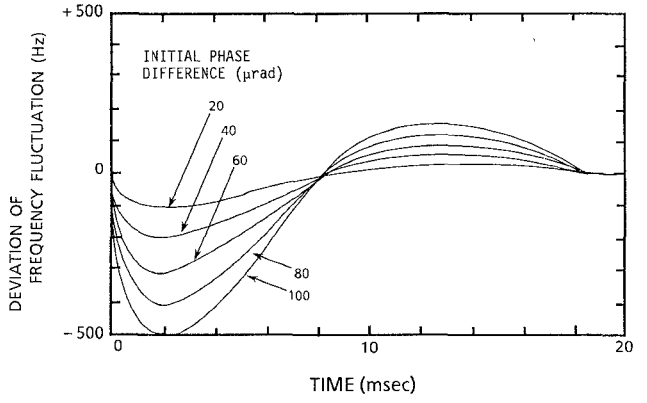

Fig. 5. Frequency response profiles for phase stepping in the 1.6 GHz band synthesizer.

Fig. 4 shows the frequency response profiles, when the phase difference is zero, as a parameter of the initial frequency difference in a conventional 1.6 GHz band synthesizer (reference signal frequency is 12.5 kHz). Fig. 5 shows the frequency response profiles, when the frequency difference is zero, as a parameter of initial phase difference in the 1.6 GHz band synthesizer.

An analysis of the frequency stepping response showed that, when the initial frequency difference is less than 300 Hz at the VCO output frequency, the deviation of frequency fluctuation after loop closure becomes gradually zero without a large frequency fluctuation.

Furthermore, in the case of the phase stepping response, when the initial phase difference is less than 50 μrad, the deviation of frequency fluctuation after the loop is closed becomes less than 300 Hz, and its phase lock establishment time[1] is less than about 1 ms.

III. Initial Phase Adjustment Technique

A SPILL frequency synthesizer using the newly developed initial-phase adjustment technique is shown in Fig. 6. For dividing the VCO signal, the SPILL synthesizer uses a

[1]Phase locking occurs when frequency fluctuation is held to less than 300 Hz.

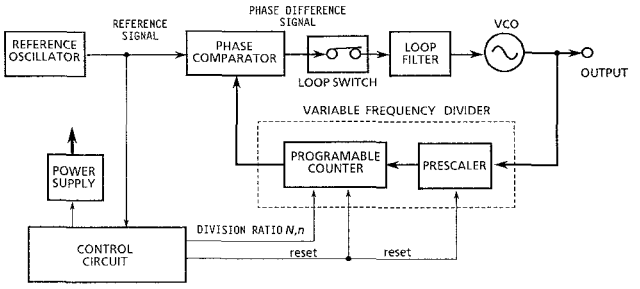

Fig. 6. SPILL frequency synthesizer using the newly developed initial-phase adjustment circuit.

resettable variable frequency divider instead of a conventional divider. Operations of this circuit consist of basic phase adjustment and precise phase adjustment.

A. Basic Phase Adjustment Operation

First, a switch is opened to maintain the VCO control voltage charged in the loop filter. Then, each circuit is put in the power-off state for a specified period. Then the variable frequency divider is reset to initialize the pulse count state. In this way, the divider is prepared to count from the initial state at the next divide operation. Power to each circuit is supplied again after a certain power-off period. Next, just before closing the loop, the basic phase adjustment is made between the two signal phases from the reference oscillator and the resettable variable frequency divider. For this operation, the count operation of the reset variable frequency divider is started, synchronously with the edge of the reference signal. If this phase adjustment is completed, it is possible to match phases within one period of the VCO output signal.

However, a delay of several tens of nanoseconds is created in the above control circuit, and this must be added to the phase difference.

B. Precise Phase Adjustment

To remove the delay time mentioned above, it is possible for the variable frequency divider's output phase to be precisely adjusted within one period of the input signal by changing the division ratio. The division ratio of the variable frequency divider is given two values, n and N, when it starts the count operation (refer to Fig. 7). N is the normal division ratio determined by the VCO output frequency, and equals the VCO output frequency divided by the reference signal frequency; n equals N minus the number Δn of VCO output frequency periods in the control circuit delay. The division ratio n is used only in the first input signal period; N is used thereafter. The phase difference resulting from the delay can be removed by this procedure. It is possible to adjust the phase difference very precisely according to the selected value n. Using this two-stage process, the maximum phase difference is approximately 50 μrad for a 1.6 GHz band frequency synthesizer with a 12.5 kHz reference signal.

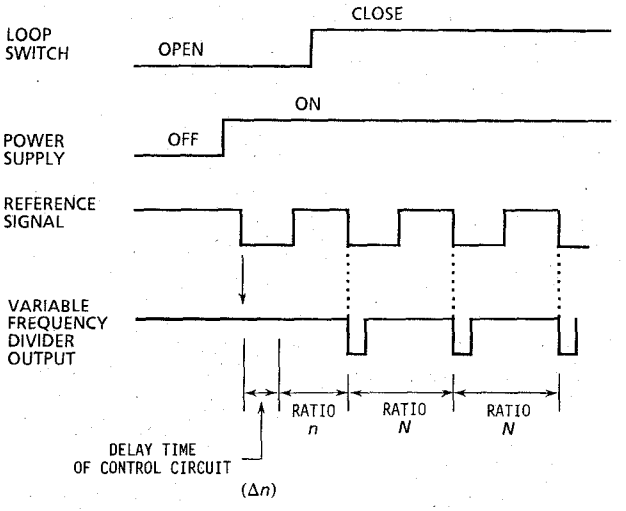

Fig. 7. Timing sequence of the newly developed initial-phase adjustment circuit.

IV. Characteristics of the Intermittent Operation

A. Experimental Circuits

The characteristics of the SPILL frequency synthesizer, consisting of an initial-phase adjustment circuit using a variable frequency divider, were examined in a laboratory experiment. In the experiment, a 1.6 GHz band frequency synthesizer was used. It consisted of a VCO generating a 1.6 GHz signal directly and a PLL circuit with a resettable variable frequency divider. The resettable variable frequency divider was composed of a pulse swallow counter with a resettable prescalar (256/258) and a programmable counter. The resettable prescaler integrated circuit was newly developed through NTT's Si process [5]. Power consumption was approximately 100 mW at 5 V and the maximum operating frequency was 2 GHz. The maximum operating frequency of the resettable prescaler can be extended to 4.5 GHz through the GaAs process [6]. Therefore, by using GaAs devices, a high-frequency synthesizer (up to 4.5 GHz) can be easily combined with the initial-phase adjustment technique.

The division ratio modifier of the above pulse swallow counter on initial phase adjustment could be easily configured only with a digital subtraction circuit, N minus Δn. First, while the variable frequency divider was in its reset status, the division ratio was adjusted by subtracting Δn from the division ratio N. Next, Δn was made zero from the positive edge of the signal at the first period and the division ratio was readjusted to N.

The quantity Δn can be derived in two ways. The simplest is to assume a fixed delay time and calculate the number of VCO output frequency periods (Δn) within the delay time. However, because of aging and temperature effects, it may not be satisfactory to treat the delay as a constant value. Therefore, the other, more powerful technique is to control Δn through an additional feedback system that measures the initial phase difference and adjust Δn to minimize the difference. This frequency synthesizer, using a resettable variable frequency divider in the 1.6 GHz band, could adjust the phase precisely within approximately 50 μrad for a 12.5 kHz reference signal.

All digital PLL circuits, excluding the prescaler, were constructed on three programmable logic cell arrays.

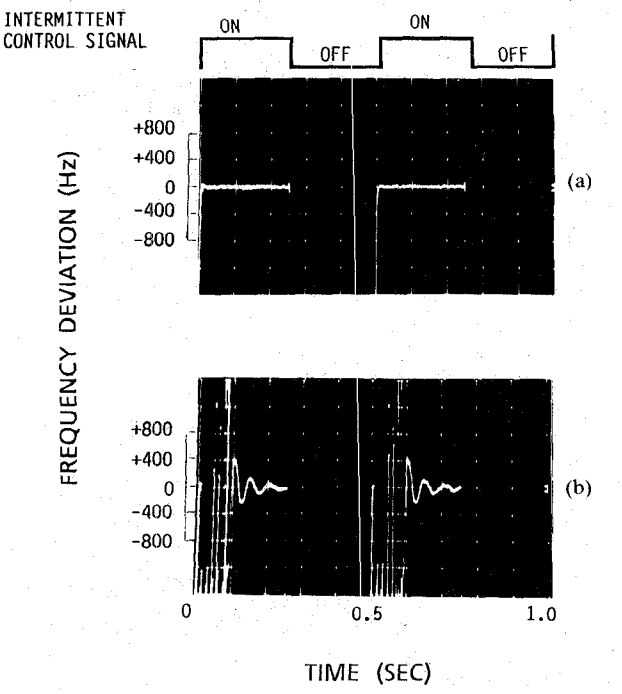

Fig. 8. VCO output frequency fluctuation when power supply to PLL circuit, including VCO, is intermittent with 1.6 GHz frequency synthesizer. (a) Initial-phase adjustment active. (b) Initial-phase adjustment inactive.

B. Intermittent Operation

Fig. 8 shows VCO output frequency fluctuation when the power supply of PLL circuit including VCO is intermittently operated. The initial phase adjustment was active in case (a) and inactive in case (b). The x axis represents time and the y axis represents frequency deviation. Frequency deviation was measured using a spectrum analyzer, whose sweep span was made 0 Hz, as a frequency discriminator. The ratio of power-on period to power-off period, ON/OFF, in the intermittent operation was 1, and each period was 250 ms. The first division ratio n of the variable frequency divider was adjusted to $n = N - 18$.

If the initial phase adjustment was inactive, the frequency stabilized within 150 ms. When the adjustment was used, the frequency stabilized within 1 ms and no frequency fluctuation could be detected. Theses results are in good agreement with theoretical estimations. Therefore, it is not necessary to supply extra power for phase locking at each intermittent period, and during each power-on period stable synthesizer output is always available. These results show that using initial-phase adjustment is more effective for reducing synthesizer power consumption than just intermittent operation.

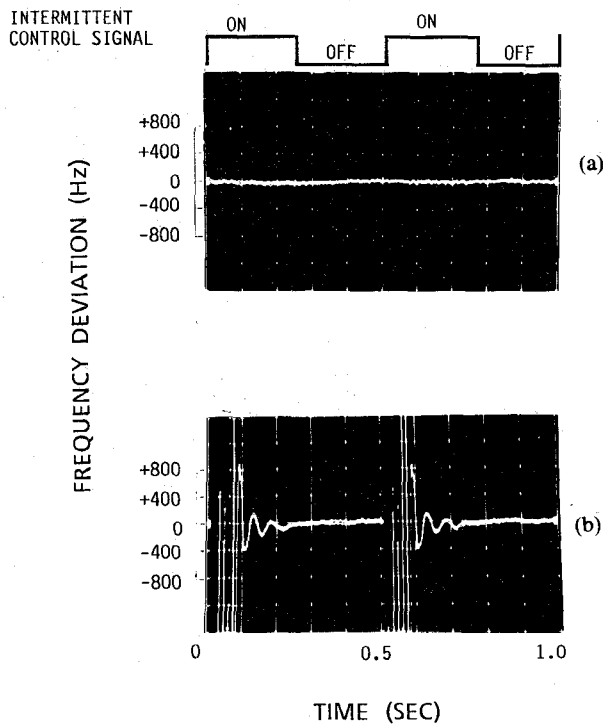

Fig. 9. VCO output frequency fluctuation when VCO is kept in the power-on state and the power suply to other PLL circuits is intermittent with 1.6 GHz frequency synthesizer. The ratio of ON/OFF is 1. (a) Initial-phase adjustment active. (b) Initial-phase adjustment inactive.

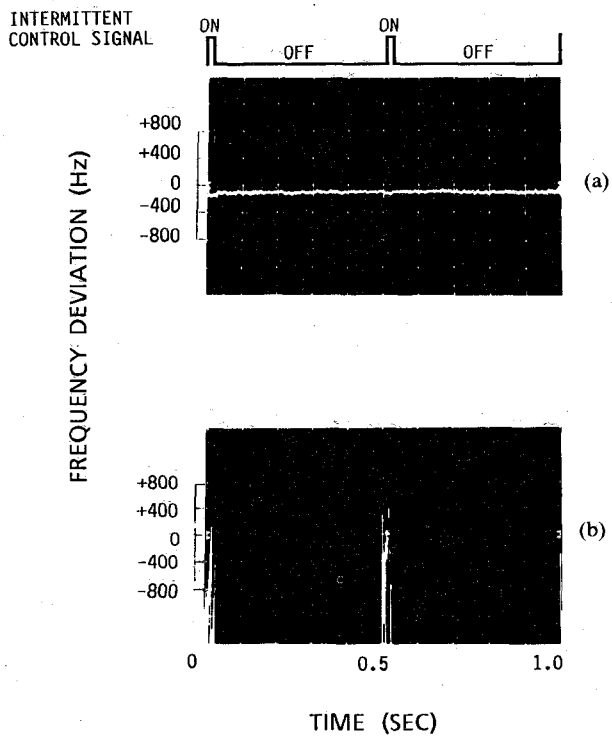

Fig. 10. VCO output frequency fluctuation when VCO is kept in power-on state and the power supply to other PLL circuits is intermittent. The ratio of ON/OFF is 1/19. (a) Initial-phase adjustment active. (b) Initial-phase adjustment inactive.

For other transceiver systems, Fig. 9 shows the VCO output frequency fluctuation when the VCO is kept in the power-on state and the power supply to the other PLL circuits is intermittent. The initial phase adjustment is used for case (a), and it is not used for case (b). The ratio of power-on period to power-off period, ON/OFF, in the intermittent operation mode was 1 and each period was 250 ms. As shown in this figure, if the initial phase adjustment is used, the PLL circuit can be operated intermittently with little frequency fluctuation. The initial phase adjustment technique is extremely stable. As shown in Fig. 10, the ratio of ON/OFF periods can be as low as 1/19 while still ensuring stable VCO output. Therefore, power consumption of the PLL circuit, including the prescaler, is expected to be reduced to 1/20 or less. The minimum ratio of ON/OFF under intermittent operation depends on the characteristics of the capacitor which holds the VCO control voltage, and period times. Power consumption can be significantly reduced by selecting a capacitor with very small leakage and decreasing the ON/OFF ratio even further. The power savings made possible through intermittent operation would be difficult, if not impossible, to duplicate with sophisticated integrated circuits.

V. Conclusion

A state-preserving intermittently locked loop (SPILL) frequency synthesizer using a resettable variable frequency divider suitable for intermittent operation to reduce power consumption has been developed. Because this frequency synthesizer maintains phase and frequency states during power-off periods, the frequency acquisition time after supplying power in the intermittent operation mode is very short. Consequently, in this mode there is very little wasted power and so this synthesizer has the great advantage of reduced power consumption.

In an experiment with a 1.6 GHz band frequency synthesizer, the acquisition time was decreased from 150 ms to less than 1 ms. In addition, the experiment on the intermittent operation of the PLL circuit, excluding the VCO, shows that power consumption of the circuit can be reduced by 95 percent or more.

This frequency synthesizer is effective in reducing the power consumption of land mobile communication systems and many kinds of communication systems using radio equipment with high-band frequency synthesizer, such as portable TV's, cordless phones, paging systems, satellite communications, and terrestrial microwave communications. Besides, the developed initial phase adjustment is also suitable for fast frequency switching.

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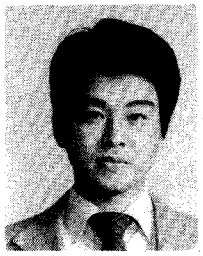

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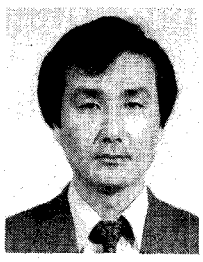

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